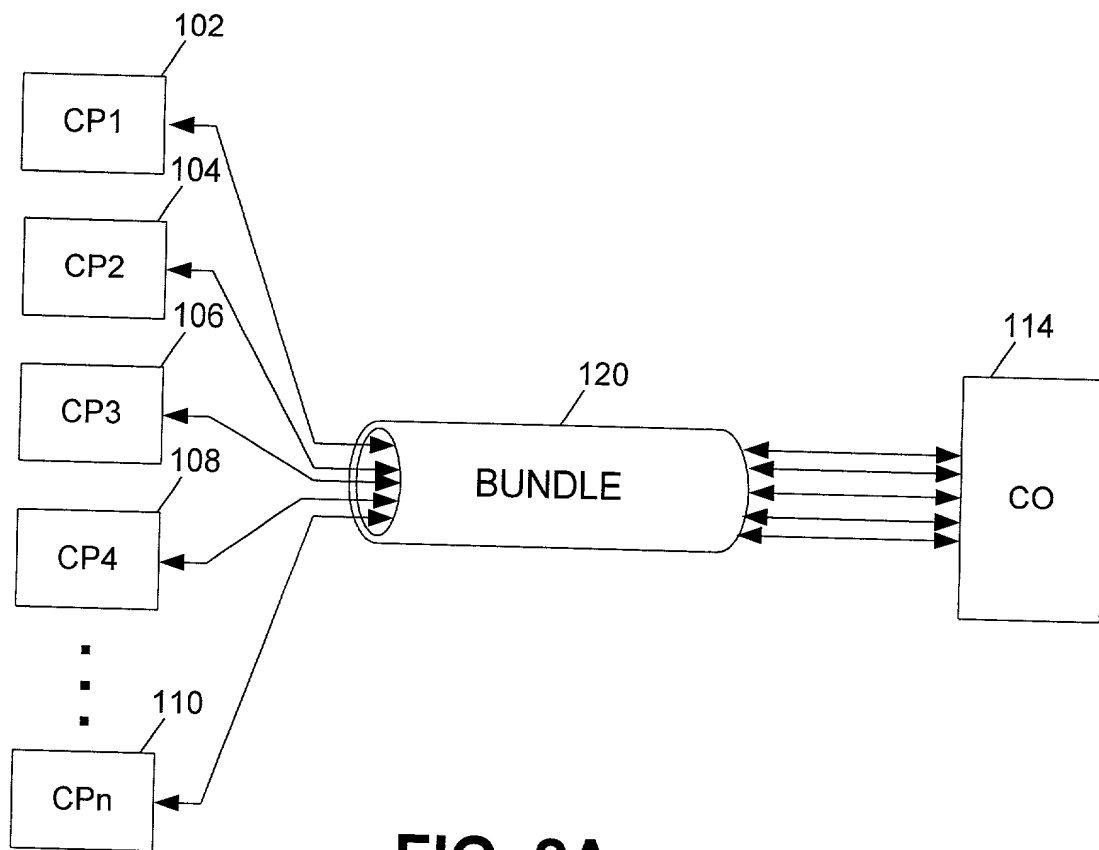
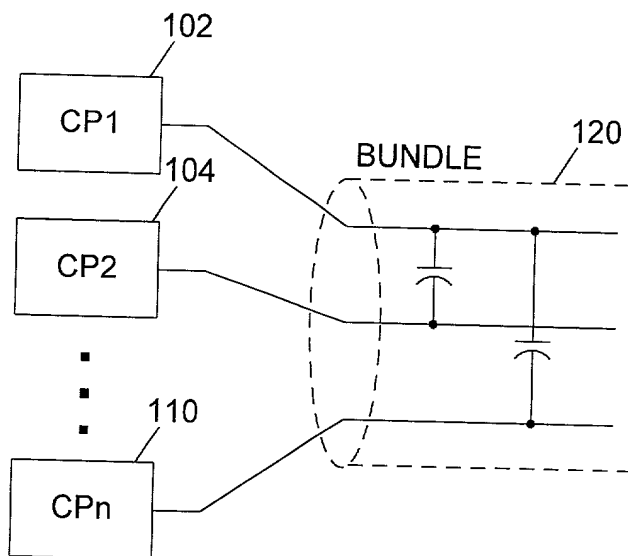


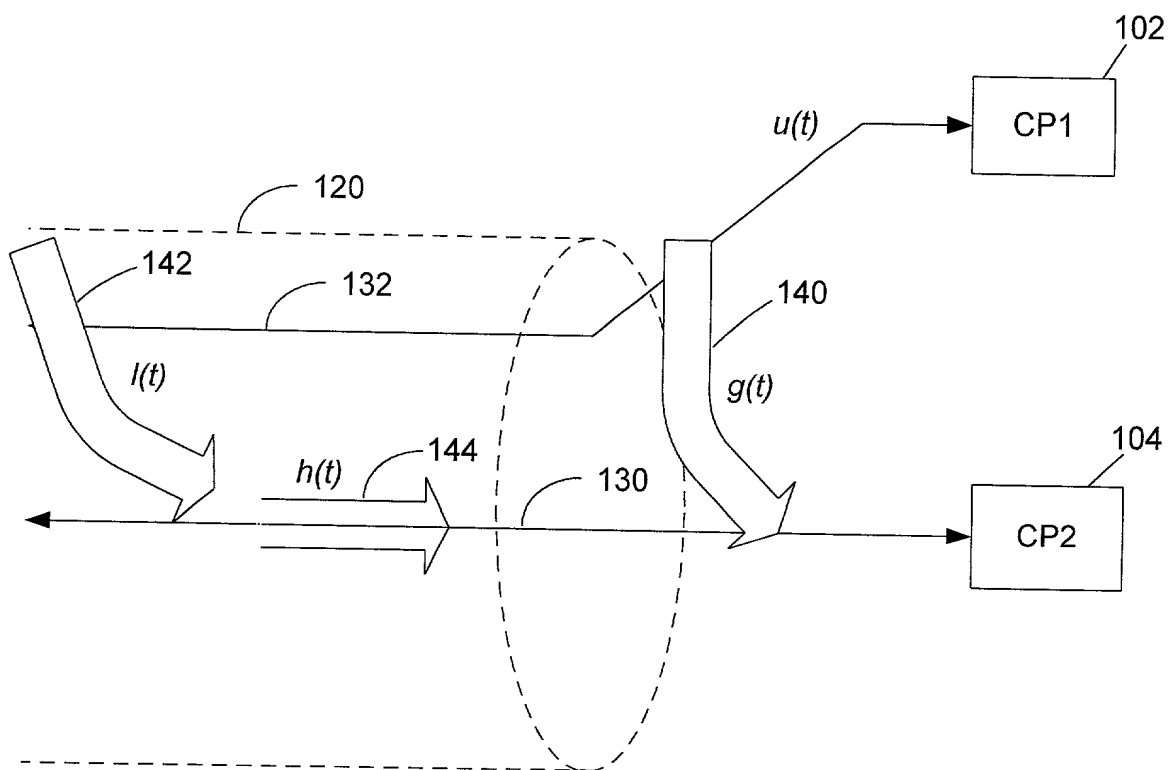
**FIG. 1 (Prior Art)**



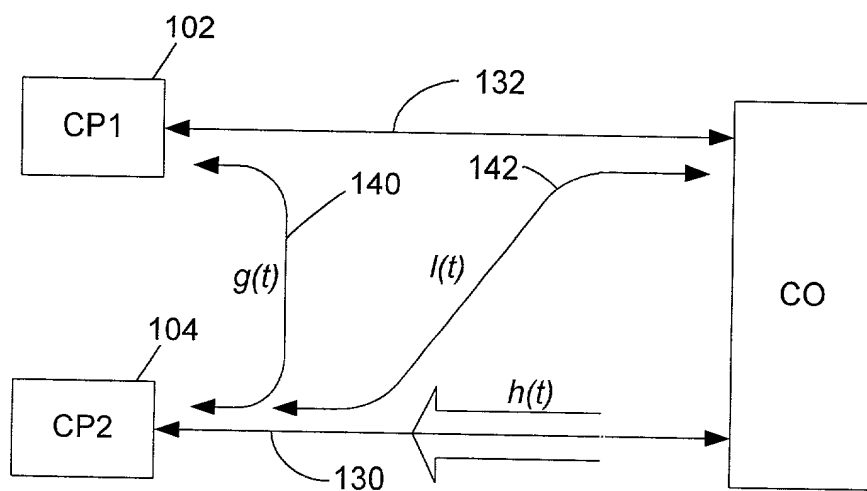
**FIG. 2A**



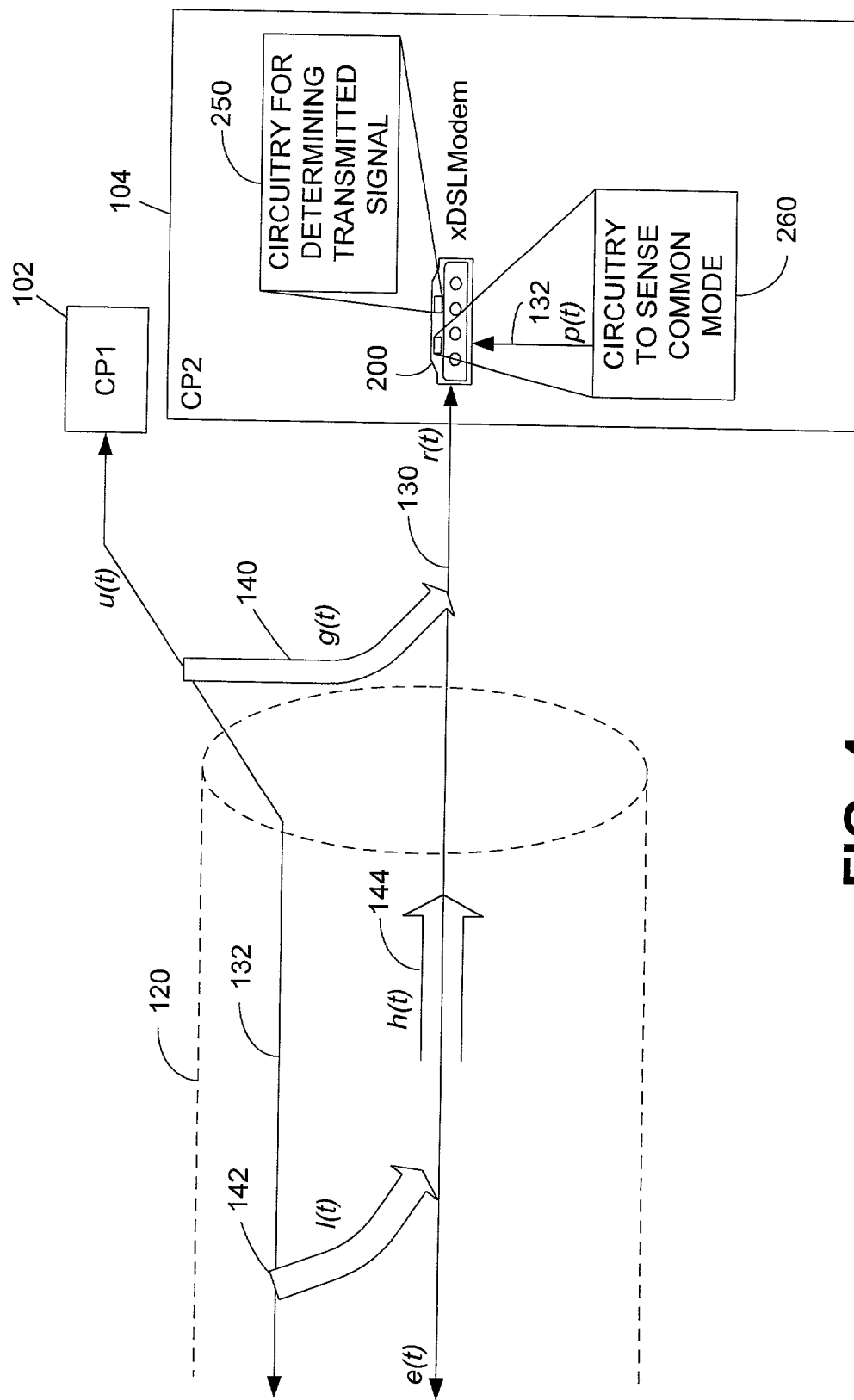
**FIG. 2B**



**FIG. 3A**



**FIG. 3B**



**FIG. 4**

DSL MODEM 200

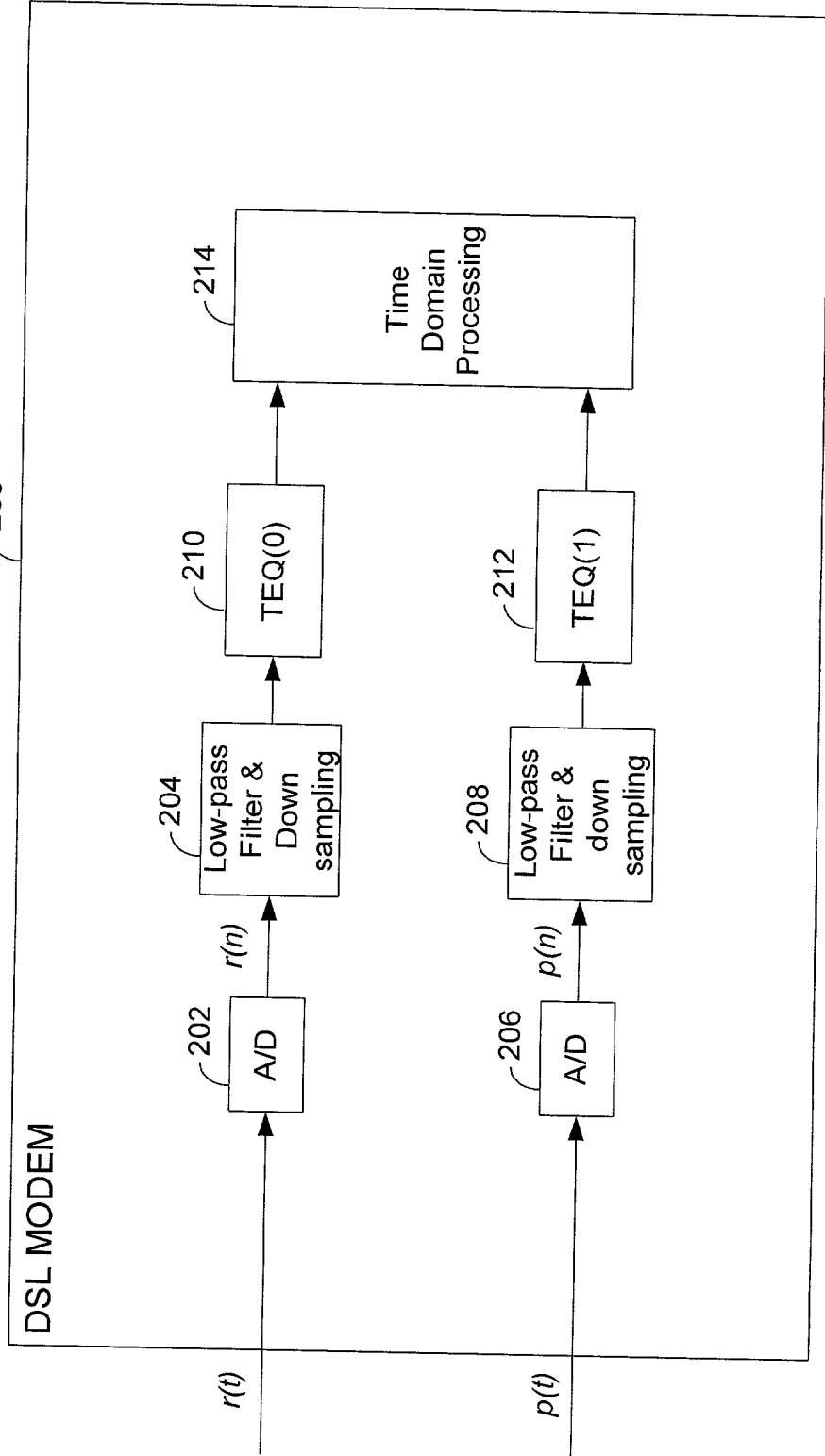


FIG. 5

FIG. 6 is a block diagram of a modem receiver 300. The receiver 300 includes two parallel processing paths for signals  $r(t)$  and  $p(t)$ . Each path consists of an A/D converter (302, 306), a low-pass filter (304, 308), a TEQ block (310, 312), an FFT block (322, 324), and a frequency domain processing block (314). The outputs of the frequency domain processing blocks are combined to produce the final output.

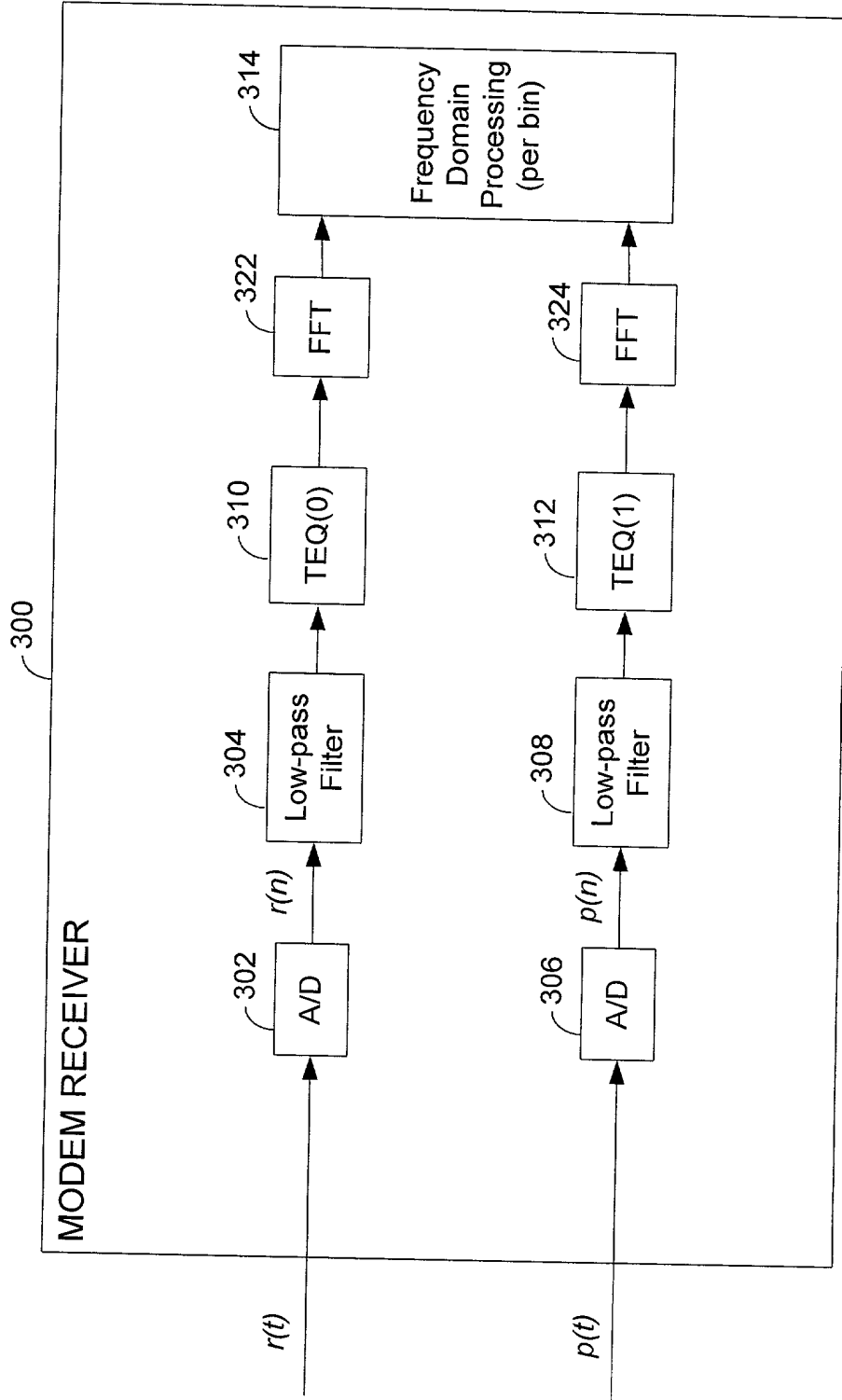
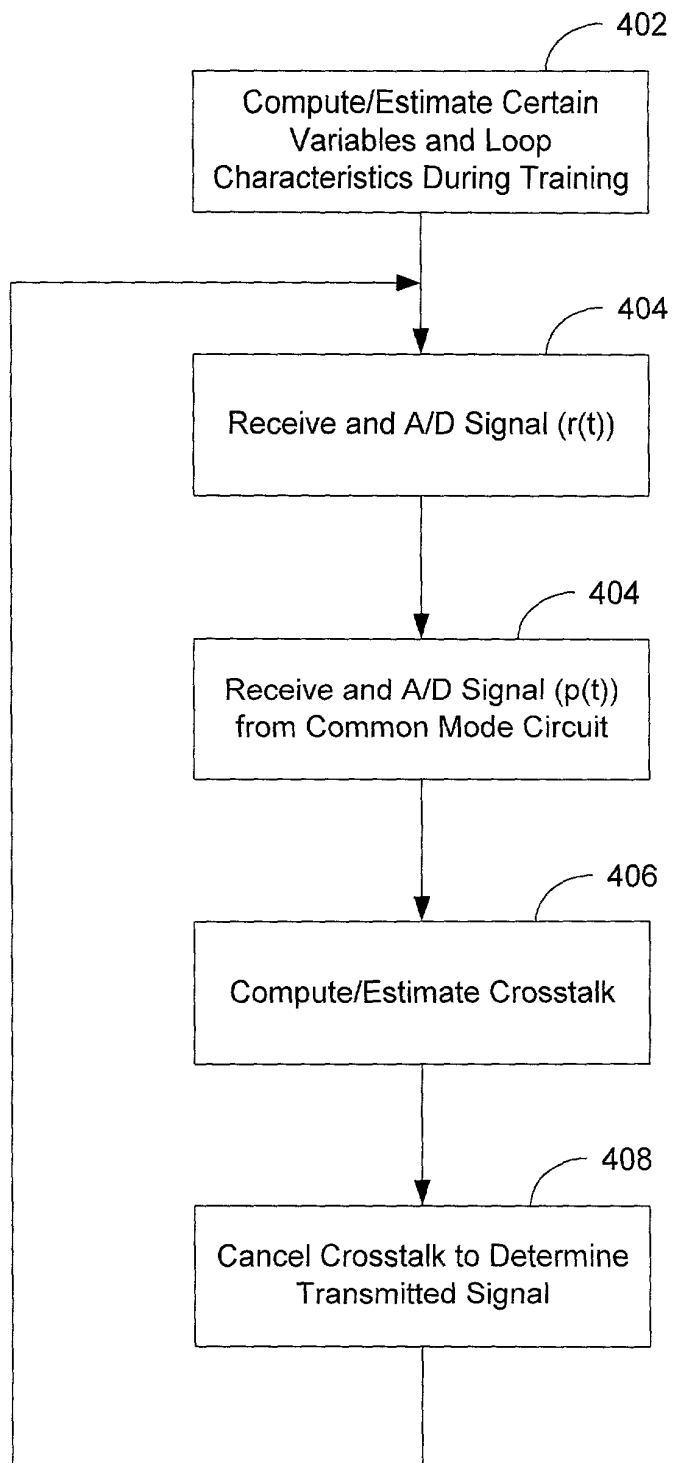
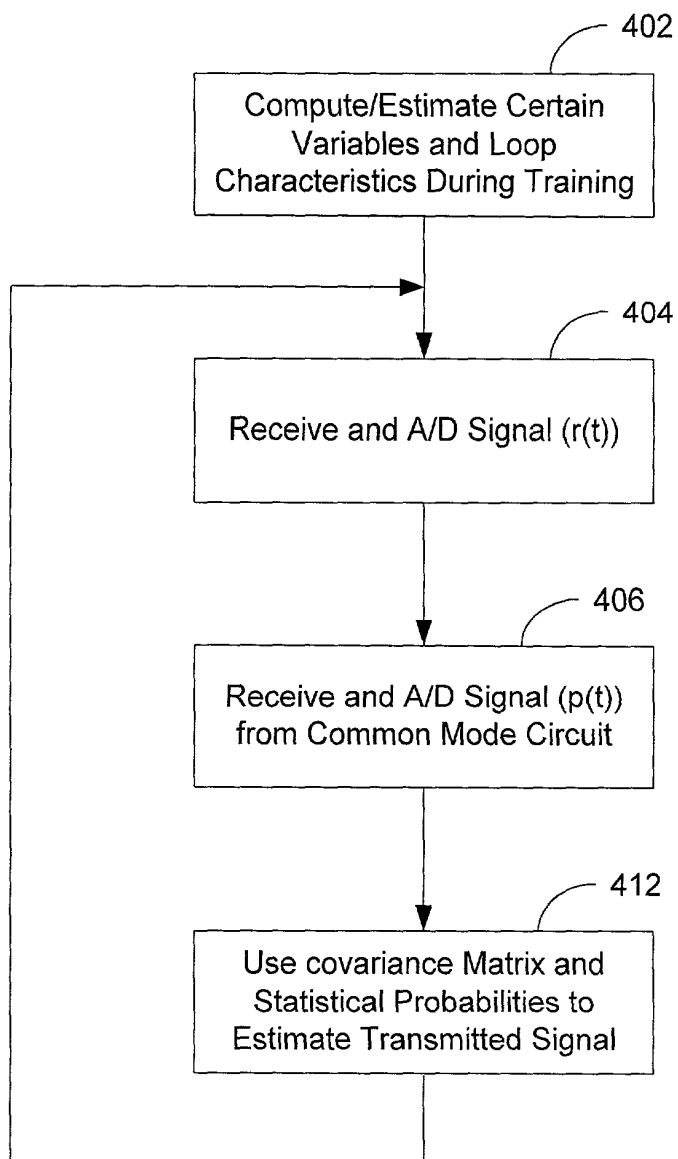


FIG. 6



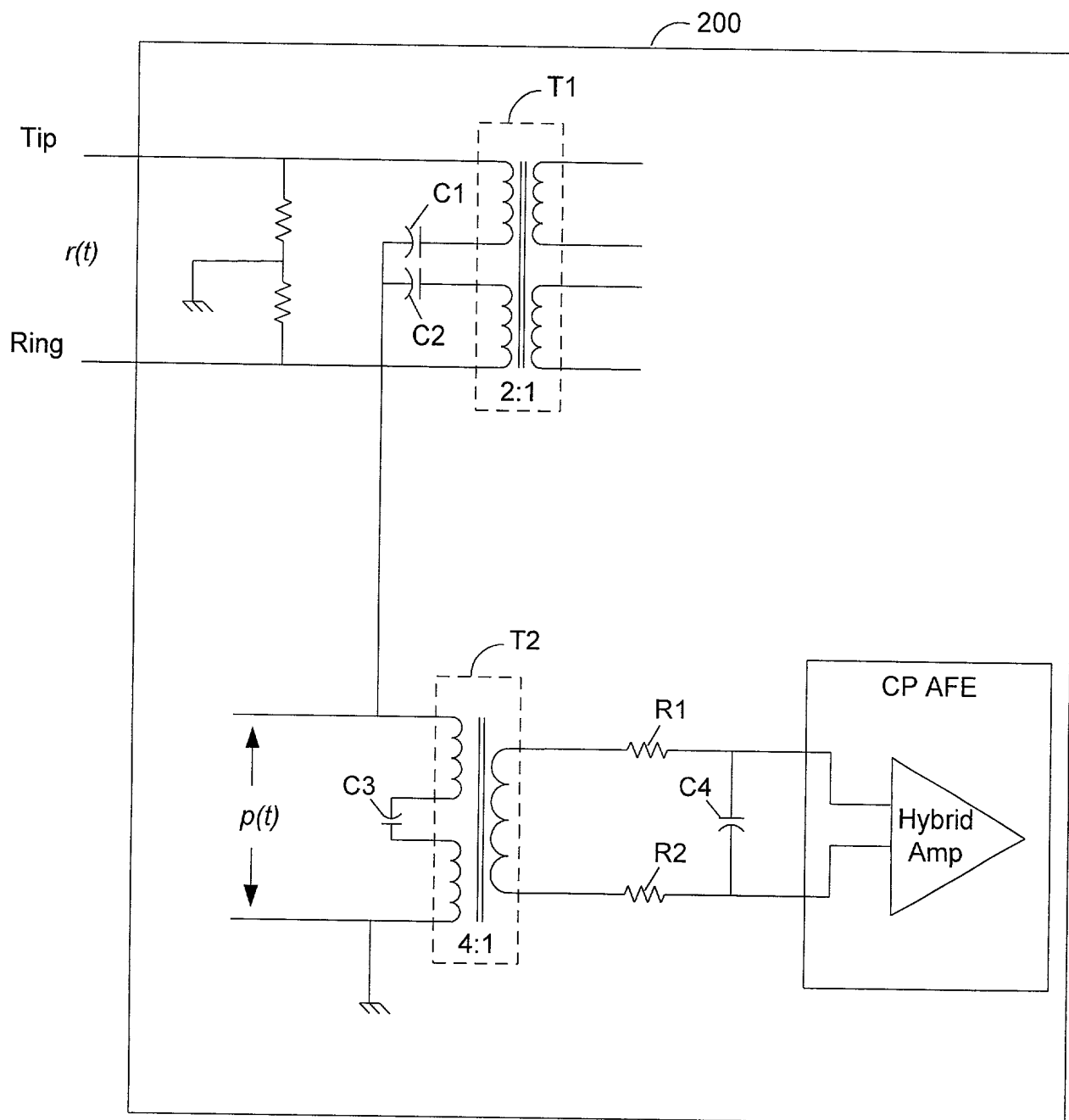
**FIG. 7**



**FIG. 8**



FIG. 9 is a schematic diagram of a system 200 for processing a signal. The system 200 includes a Tip and a Ring input. The Tip input is connected to a resistor network and a transformer T1. The Ring input is connected to a resistor network and a transformer T1. The transformer T1 has a 2:1 turns ratio. The output of T1 is connected to a capacitor C1 and a capacitor C2. The output of C1 and C2 is connected to a transformer T2. The transformer T2 has a 4:1 turns ratio. The output of T2 is connected to a resistor network (R1, R2) and a capacitor C4. The output of R1, R2, and C4 is connected to a CP AFE (Control Plane Analog Front End) block. The CP AFE block includes a Hybrid Amp. The output of the Hybrid Amp is connected to a signal p(t).



**FIG. 9**